COM232/4PC

Four Channel Asynchronous Serial Communications Adapter

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COM232/4PC
User's Manual

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Table of Contents

1.1 Introduction

The COM232/4PC is a four channel RS-232 asynchronous serial communication adapter. The adapter is designed to be hardware compatible with the IBM PC/XT/AT personal computers. Data is communicated through a D-37 shielded connector which provides greater shielding against environmental noise. A D-37 to four D-25 converter cable is included to produce four "standard" 25-pin RS-232 interfaces.

The serial interface is accomplished through four 16450 Asynchronous Communication Elements (ACEs). The 16450 is an improved specification version of the 8250 ACEs used in the IBM PC/XT models. Optional 16550 ACEs are available to reduce CPU overhead at higher data rates when used with software supporting this feature.

Addressing for the adapter is selected by a pair of six position switches. These switches allow a full range of address choices between 0 and FFFF hex. The COM232/4PC has the option of selecting one of six possible Interrupt Request lines (IRQ 2 - IRQ 7). A hardware selectable clock divider is also available for producing unusual baud rates.

NOTE

The optional 16550 ACE has been installed within your IOtech COM232/4PC board.

1.2 Board Description

The first channel of the COM232/4PC is controlled by the ACE labeled U9, switches SW1 & SW2 for addressing, jumper J10 for interrupts, and jumper J2 for signal assignment. Channel 1 is accessed through the RJ-11 connector labeled CON1.

The remaining seven channels and their corresponding signal-assignment jumpers are as follows: Channel 2 is labeled U14 with jumper J3, Channel 3 is labeled U10 with jumper J4, Channel 4 is labeled U15 with jumper J5, Channel 5 is labeled U11 with jumper J6, Channel 6 is labeled U16 with jumper J7, Channel 7 is labeled U12 with jumper J8, and Channel 8 is labeled U17 with jumper J9. The address of each of the ports are incremented by a factor of 8 in hexadecimal code. In other words, if Channel 1 was at a address of 0300H, Channel 2 would be at 0308H. The input clock frequency is controlled by jumper J1.

1.3 Specifications

Bus interface: IBM 8-bit bus (PC/XT)

Dimensions: 10.75"x3.9"

Controllers: 4 - 16450 Asynchronous Communication Elements

Transmit drivers: MC1488 or compatible

Receive buffers: MC1489 or compatible

RS-232 interface: 1 - D-37 connectors (female)

Optional: 4 - D-25 connectors (male) using adapter cable provided

I/O Address range: See Section 1.7

Interrupt levels: IRQ 2(9),3-7

Power requirements:

I_T	I_{MS}	Supply
382mA	438 mA	+5 Volts
57mA	67mA	+12 Volts
54mA	63mA	-12 Volts

I_T - Typical adapter current

I_{MS} - Maximum statistical adapter current

1.4 16450/16550 Functional Description

The 16450 is an improved specification version of the 8250 Asynchronous Communications Element (ACE). Functionally, the 16450 is equivalent to the 8250. The ACE performs serial-to-parallel conversion on received data and parallel-to-serial conversion on data output from the CPU.

Designed to be compatible with the 16450, the 16550 ACE enters character mode on reset and in this mode appears as a 16450 to user software. An additional mode, FIFO mode, can be invoked through software to reduce CPU overhead. The FIFO mode increases performance by providing two 16-byte FIFOs (one transmit and one receive) to buffer data and reduce the number of interrupts issued to the CPU.

Other features of the 16450/16550 include:

- Programmable baud rate, character length, parity, and number of stop bits.
- Automatic addition and removal of start, stop, and parity bits.

- Independent and prioritized transmit, receive and status interrupts.
- Transmitter clock output to drive receive logic.
- External receiver clock input.

The following pages provide a brief summary of the internal registers available within the 16450 and 16550 ACEs. The registers are addressed as shown in figure 1 below. Registers specific to the 16550 will be marked with an asterisk(*). NOTE: DLAB is accessed through the Line Control Register.

DLAB	A2	A1	A0	Register Description
0	0	0	0	Receive buffer (read only) Transmit holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only) FIFO control* (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (LSB)
1	0	0	1	Divisor latch (MSB)

Figure 1: Internal Register Map for 16450 & 16550 ACEs

1.4.1 Interrupt Enable Register

The bit definitions for this register are as follows:

D7	0	
D6	0	
D5	0	
D4	0	
D3	EDSSI	MODEM Status
D2	ELSI	Receiver Line Status
D1	ETBEI	Trans. Holding Register Empty
D0	ERBFI	Received Data Available

Figure 2: Interrupt Enable Register Definitions

EDSSI MODEM Status Interrupt:	When set (logic 1), enables interrupt on clear to send, data set ready, ring indicator, and data carrier detect.
ELSI Receiver Line Status Interrupt:	When set (logic 1), enables interrupt on overrun, parity, framing errors, and break indication.
ETBEI Transmitter Holding Register Empty Interrupt:	When set (logic 1), enables interrupt on transmitter register empty.
ERBFI Received Data Available Interrupt:	When set (logic 1), enables interrupt on received data available or FIFO trigger level.

* For Optional 16550 only.

1.4.2 Interrupt Identification Register

The bit definitions for this register as as follows:

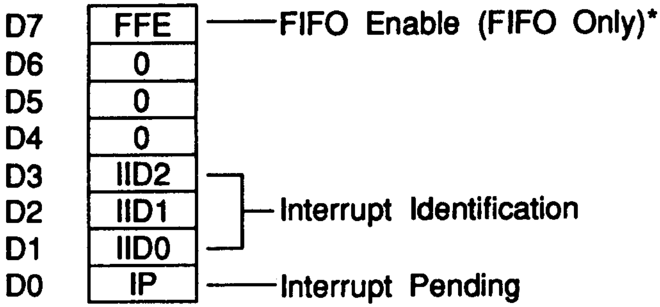


Figure 3: Interrupt Identification Register Definitions

FFE FIFO Enable:*	When logic 1, indicates FIFO mode enabled. .
IIDx Interrupt Identification:	Indicates highest priority interrupt pending if any. See IP and figure 5. NOTE: IID2 is always a logic 0 in the character mode.
IP Interrupt Pending:	When logic 0, indicates that an interrupt is pending and the contents of the interrupt identification register may be used to determine the interrupt source. See IIDx and figure 4.

* For Optional 16550 only.

IID2	IID1	IID0	IP	Priority	Interrupt Type
x	x	x	1	N/A	None
0	1	1	0	Highest	Receiver Line Status
0	1	0	0	Second	Received Data Ready
1	1	0	0	Second	Character Timeout* (FIFO only)
0	0	1	0	Third	Transmitter Holding Register Empty
0	0	0	0	Fourth	MODEM Status

Figure 4: Interrupt Identification Bit Definitions

Receiver Line Status:	Indicates overrun, parity, framing errors or break interrupts. The interrupt is cleared by reading the line status register.
Received Data Ready:	Indicates receiver data available. The interrupt is cleared by reading the receiver buffer register.
FIFO mode:*	Indicates the receiver FIFO trigger level has been reached. The interrupt is reset when the FIFO drops below the trigger level.
Character Timeout:* (FIFO mode only)	Indicates no characters have been removed from or input to the receiver FIFO for the last four character times and there is at least one character in the FIFO during this time. The interrupt is cleared by reading the receiver FIFO.
Transmitter Holding Register Empty:	Indicates the transmitter holding register is empty. The interrupt is cleared by reading the interrupt identification register or writing to the transmitter holding register.
MODEM Status:	Indicates clear to send, data set ready, ring indicator, or data carrier detect have changed state. The interrupt is cleared by reading the MODEM status register.

* For Optional 16550 only.

1.4.3 FIFO Control Register

For Optional 16550 Only

The bit definitions of this register are as follows:

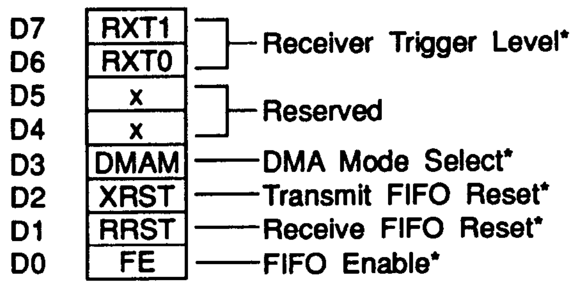


Figure 5: FIFO Control Register

RXTx - Receiver FIFO Trigger Level:*	Determines the trigger level for the FIFO interrupt as given in the table below.

RXT1	RXT0	Trigger Level (bytes)
0	0	1
0	0	4
1	0	8
1	1	14

Figure 6: FIFO Trigger Levels

DMAM DMA Mode Select:*	When set (logic 1), RxRDY and TxRDY change from mode 0 to mode 1 for DMA transfers. DMA mode is not supported on COM232/4PC.
XRST Transmit FIFO Reset:*	When set (logic 1), all bytes in the transmitter FIFO are cleared and the counter is reset. The shift register is not cleared. XRST is self-clearing.

RRST Receive FIFO Reset:*	When set (logic 1), all bytes in the receiver FIFO are cleared and the counter is reset. The shift register is not cleared. RRST is self-clearing.
FE FIFO Enable:*	When set (logic 1), enables transmitter and receiver FIFOs. When cleared (logic 0), all bytes in both FIFOs are cleared. This bit must be set when other bits in the FIFO control register are written to or the bits will be ignored.

* For Optional 16550 only.

1.4.4 Line Control Register

The bit definitions for this register are as follows:

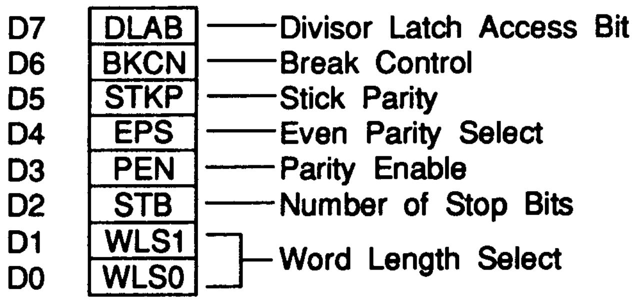


Figure 7: Line Control Register

DLAB Divisor Latch Access Bit:	DLAB must be set to logic 1 to access the baud rate divisor latches. DLAB must be set to logic 0 to access the receiver buffer, transmitting holding register and interrupt enable register.
BKCN Break Control:	When set (logic 1), the serial output (SOUT) is forced to the spacing state (logic 0).
STKP Stick Parity:	Forces parity to logic 1 or logic 0 if parity is enabled. See EPS, PEN, and Figure 8.
EPS Even Parity Select:	Selects even or odd parity if parity is enabled. See STKP, PEN, and Figure 8.

PEN Parity Enable:	Enables parity on transmission and verification on reception. See EPS, STPK, and figure 8.

STKP	EPS	PEN	Parity
x	x	0	None
0	0	1	Odd
0	1	1	Even
1	0	1	Logic 1
1	1	1	Logic 2

Figure 8: 16450/16550 Parity Selections

STB Number of Stop Bits:	Sets the number of stop bits transmitted. See WLSx and Figure 9.
WLSx Word Length Select:	Determines the number of bits per transmitted word. See STB and Figure 9.

STB	WLS1	WLS0	Word Length	Stop Bits
0	0	0	5 bits	1
0	0	1	6 bits	1
0	1	0	7 bits	1
0	1	1	8 bits	1
1	0	0	5 bits	1 1/2
1	0	1	6 bits	2
1	1	0	7 bits	2
1	1	1	8 bits	2

Figure 9: Word Length and Stop Bit Selections

1.4.5 Modem Control Register

The bit definitions for this register are as follows:

Bit	Value	Definition
D7	0	
D6	0	
D5	0	
D4	LOOP	Loopback Enable
D3	OUT2	Output 2
D2	OUT1	Output 1
D1	RTS	Request to Send
D0	DTR	Data Terminal Ready

Figure 10: MODEM Control Register Definitions

LOOP Loopback Enable:	When set (logic 1), the transmitter shift register is connected directly to the receiver shift register. The MODEM control inputs are internally connected to the MODEM control outputs and the outputs are forced to the inactive state. Therefore all characters transmitted are immediately received to verify transmit and receive data paths. Transmitter and receiver interrupts still operate normally. MODEM control interrupts are available but are now controlled through the MODEM control register.

Bits OUT2, OUT1, RTS, and DTR perform identical functions on their respective outputs. When these bits are set (logic 1) in the register, the associated output is forced to a logic 0. When cleared (logic 0), the output is forced to a logic 1.

OUT2 Output 2:	Controls the OUT2 output as described above.
OUT1 Output 1:	Controls the OUT1 output as described above.
RTS Request To Send:	Controls the RTS output as described above.

DTR Data Terminal Ready:	Controls the DTR output as described above.

1.4.6 Line Status Register

The bit definitions for this register are as follows:

D7	FFRX	Error in FIFO RCVR (FIFO Only)*
D6	TEMT	Transmitter Empty
D5	THRE	Transmitter Holding Register Empty
D4	BI	Break Interrupt
D3	FE	Framing Error
D2	PE	Parity Error
D1	OE	Overrun Error
D0	DR	Data Ready

Figure 11: Line Status Register Definitions

FFRX FIFO Receiver Error:*	Always a logic 0 in character mode.
FIFO mode:	Indicates one or more parity errors, framing errors, or break indications in the receiver FIFO. FFRX is reset by reading the line status register.
TEMT Transmitter Empty:	Indicates the transmitter holding register (or FIFO*) and the transmitter shift register are empty and are ready to receive new data. TEMT is reset by writing a character to the transmitter holding register.
THRE Transmitter Holding Register Empty:	Indicates the transmitter holding register (or FIFO*) is empty and it is ready to accept new data. THRE is reset by writing data to the transmitter holding register.

* For Optional 16550 only.

Bits BI, FE, PE, and OE are the sources of receiver line status interrupts. The bits are reset by reading the line status register. In FIFO mode , these bits are associated with a specific character in the FIFO and the exception is revealed only when that character reaches the top of the FIFO.

BI Break Interrupt:	Indicates the receive data input has been in the spacing state (logic 0) for longer than one full word transmission time.
FIFO mode:*	Only one zero character is loaded into the FIFO and transfers are disabled until SIN goes to the mark state (logic 1) and a valid start bit is received.
FE Framing Error:	Indicates the received character had an invalid stop bit. The stop bit following the last data or parity bit was a 0 bit (spacing level).
PE Parity Error:	Indicates that the received data does not have the correct parity.
OE Overrun Error:	Indicates the receive buffer was not read before the next character was received and the character is destroyed.
* FIFO mode:	Indicates the FIFO is full and another character has been shifted in. The character in the shift register is destroyed but is not transferred to the FIFO.
DR Data ready:	Indicates data is present in the receive buffer (or FIFO). DR is reset by reading the receive buffer register or receiver FIFO.

* For Optional 16550 only.

1.4.7 Modem Status Register

The bit definitions for this register are as follows:

D7	DCD	Data Carrier Detect
D6	RI	Ring Indicator
D5	DSR	Data Set Ready
D4	CTS	Clear to Send
D3	DDCD	Delta Data Carrier Detect
D2	TERI	Trailing Edge Ring Indicator
D1	DDSR	Delta Data Set Ready
D0	DCTS	Data Clear to Send

Figure 12: MODEM Status Register Definitions

DCD Data Carrier Detect:	Complement of the DCD input.
RI Ring Indicator:	Complement of the RI input.
DSR Data Set Ready:	Complement of the DSR input.
CTS Clear To Send:	Complement of the CTS input.

Bits DDCD, TERI, DDSR, and DCTS are the sources of MODEM status interrupts. These bits are reset when the MODEM status register is read.

DDCD Delta Data Carrier Detect:	Indicates the Data Carrier Detect input has changed state.
TERI Trailing Edge Ring Indicator:	Indicates the Ring Indicator input has changed from a low to a high state.
DDSR Delta Data Set Ready:	Indicates the Data Set Ready input has changed state.
+DCTS Delta Clear To Send:	Indicates the Clear to Send input has changed state.

1.4.8 Scratchpad Register

This register is not used by the 16450 or 16550 ACEs. It may be used by the programmer for data storage.

1.5 FIFO Interrupt Mode Operation

For Optional 16550 Only

1. The receive data interrupt is issued when the FIFO reaches the trigger level. The interrupt is cleared as soon as the FIFO falls below the trigger level.
2. The interrupt identification register's receive data available indicator is set and cleared along with the receive data interrupt above.
3. The data ready indicator is set as soon as a character is transferred into the receiver FIFO and is cleared when the FIFO is empty.

1.6 Baud Rate Selection

The 16450 ACE determines the baud rate of the serial output using a combination of the input clock frequency and the values contained in the divisor latches. Standard PC, PC/XT, PC/AT, and PS/2 serial interfaces use an input clock of 1.8432 Mhz. To increase versatility, the COM232/4PC uses an 18.432 Mhz crystal and a frequency divider circuit to produce the standard clock frequency.

Jumper block J1 is used to set the frequency input to the 16450. It may be connected to divide the clock input by 1, 2, 5, or 10. For compatibility, J1 should be configured to divide by 10 as shown in figure 13(d). A table of baud rates available using the 1.8432 Mhz input is given in figure 14.

* For Optional 16550 only.

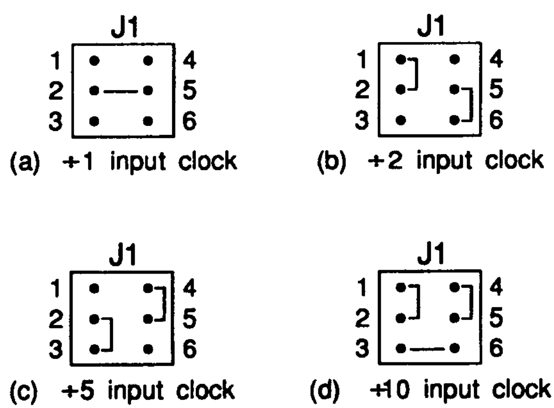


Figure 13: Input Clock Frequency Options

NOTE: For compatibility, the jumper should be set at +10 (18.432 Mhz +10 = 1.8432 Mhz). The following table lists divisor latch settings for common baud rates using an 1.8432 Mhz input clock. For compatibility, connect jumper in the divide by 10 configuration (figure 13(d)).

Desired Baud Rate	Divisor Latch Value	Error Between Desired and Actual Value (5)
50	2304	—
75	1536	—
110	1047	0.026
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

Figure 14: Divisor Latch Settings

1.7 Addressing

The COM232/4PC uses 8 I/O address locations per channel. Full sixteen bit address decoding allows base address selections in the range 0000 - FFFF Hex. Two six position switches, SW1 & SW2 are used to specify the base address of the adapter. SW1 controls the address setting for A15-A10 through positions 1-6 respectively. Switch SW2, positions 1-5 control address selections for A9-A5. The remaining address inputs are used by the adapter to determine the channel and register being accessed.

A switch in the "ON" position indicates that the corresponding address bit be a logic 0 for selection. A switch in the "OFF" position forces the corresponding address bit to be a logic 1 for selection. Some example switch settings for the COM232/4PC are shown in figures 15 and 16.

The base address of each channel is incremented by a factor of 8 from the base address of the adapter. Therefore, 32 address locations are used by the COM232/4PC.

Port	Address Range
1	Base Address+0 - Base Address+7
2	Base Address+8 - Base Address+15
3	Base Address+16 - Base Address+23
4	Base Address+24 - Base Address+31

The figure below shows an address selection of channel 1. The address is set for 0300H.

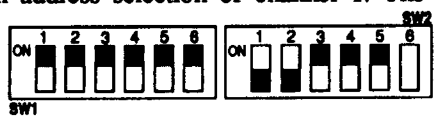


Figure 15: Factory Address Switch Settings

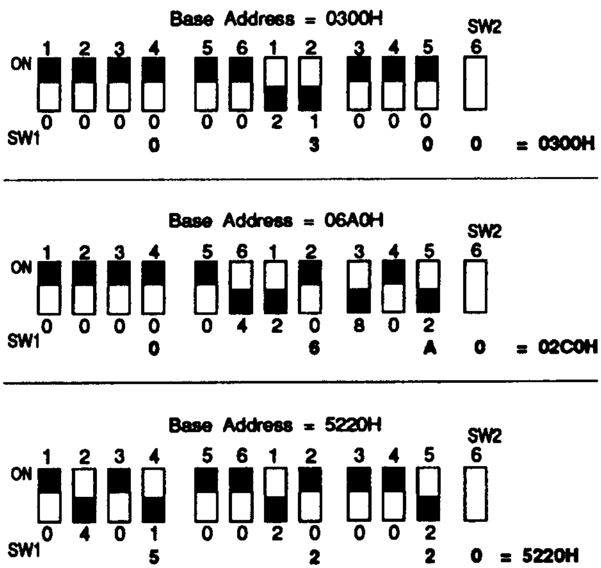


Figure 16: Address Switch Selection Examples

1.8 Interrupts

The COM232/4PC is capable of supporting six interrupt levels, IRQ 2-7. All of the channels share the same interrupt. The selection of interrupt levels can be changed through a hardware jumper, J6, as shown below:

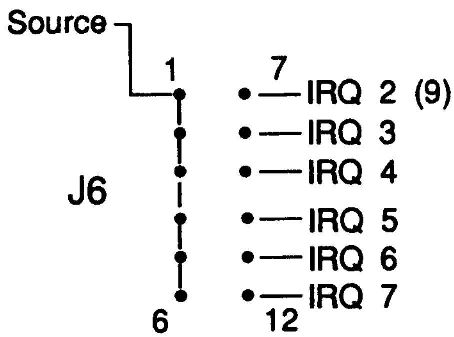


Figure 17: Interrupt Level Selection Jumper

The COM232/4PC is also equipped with an interrupt sharing circuit. This circuit allows the COM232/4PC to share its interrupt with other IOtech adapters supporting this feature.

1.8.1 Interrupt Status Register Select

An interrupt status register is implemented on the COM232/4PC to reduce the interrupt servicing overhead associated with multi-port communications. Scratchpad/ Interrupt Status register selection is controlled by position 6 on SW2. When position 6 is in the OFF position, there is no Interrupt Status register, and all of the 16450/16550s behave normally. When position 6 is in the ON position, the Interrupt Status register over-rides the 16450/16550's internal Scratchpad register. In this mode, an input from the Scratchpad register address (BASE ADDRESS + 7) of any channel will return the interrupt status of the entire card.

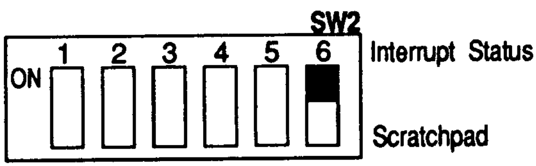


Figure 18: Scratchpad/Interrupt Status Select

IPx set, indicates an interrupt is pending on the associated channel.

D7	0
D6	0
D5	0
D4	0
D3	IP4
D2	IP3
D1	IP2
D0	IP1

Figure 19: Interrupt Status Register

1.9 Output Configurations

1.9.1 RS-232

RS-232-C devices are classified by their function as either Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). Generally, data terminal equipment is defined as the communication source while data communication equipment is defined as devices that provide a communication channel between two DTE type devices.

The figure below shows the use of Data Terminal Equipment (DTE) and Data Communication Equipment (DCE) to implement an RS-232-C communication link.

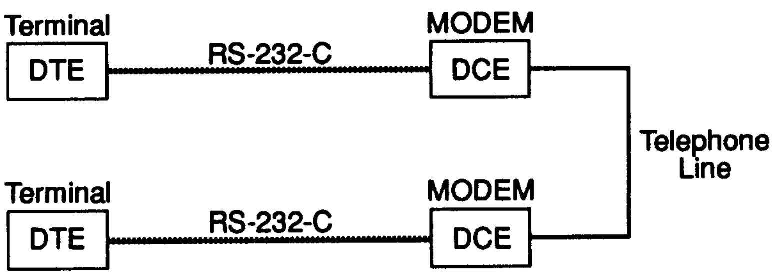
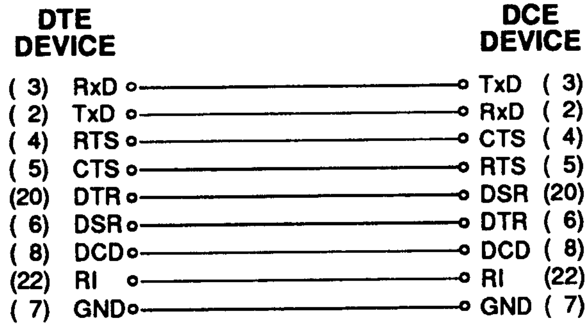
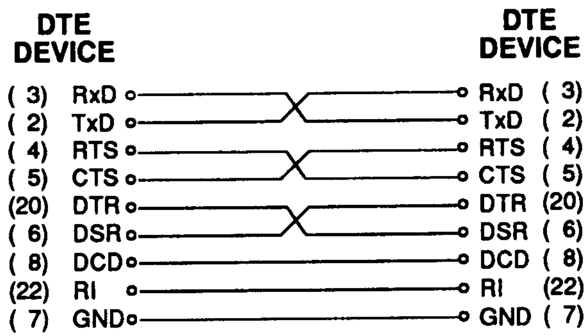


Figure 20: RS-232-C Communication Link

Data terminal equipment and data communication equipment have complementary pinouts to allow terminals and MODEMs to be connected directly using a one-to-one cable as shown in the top figure below. In many applications, DCEs are unnecessary because of the short distances involved. In these cases, a custom cable called a NULL MODEM or MODEM eliminator is usually required to perform the direct connection of two DTEs. A typical null MODEM cable is shown below in the bottom figure.



Typical DTE to DCE Cable



Typical DTE to DTE Cable (null MODEM)

Figure 21: Cabling Requirements for RS-232 Devices

1.9.2 External Connections

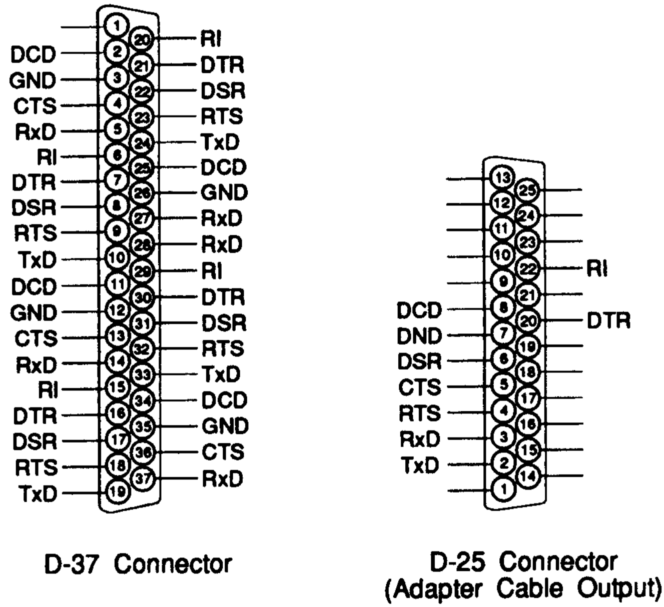


Figure 22: Output Connectors

	CHANNEL 1		CHANNEL 2		CHANNEL 3		CHANNEL 4	
SIGNAL	**D-37**	**D-25**	**D-37**	**D-25**	**D-37**	**D-25**	**D-37**	**D-25**
TxD	24	2	10	2	33	2	19	2
RxD	5	3	28	3	14	3	37	3
RTS	23	4	9	4	32	4	18	4
CTS	4	5	27	5	13	5	36	5
DTR	21	20	7	20	30	20	16	20
DSR	22	6	8	6	31	6	17	6
DCD	2	8	25	8	11	8	34	8
RI	20	22	6	22	29	22	15	22
GND	3	7	26	7	12	7	35	7

Figure 23: Connector Assignments

1.10 Hardware Installation

1. Set addressing, interrupts and output configuration jumpers on the card.
2. Turn unit off.
3. Remove system cover as instructed in the computer reference guide.
4. Insert card into a vacant slot following the guidelines for installation.
5. Replace system cover.

1.11 Software Installation

1.11.1 DOS Installation

This section briefly describes some of the files contained on the installation disk. Particularly:

- COMDRIVE.SYS
- QMODE.COM
- QCFG.EXE

The files on this disk are intended to be used with IOtech's multi-port ASYNC boards.

COMDRIVE.SYS

This program is installed with CONFIG.SYS and should be located at [C:\COMDRIVE.SYS]. COMDRIVE allows for the use of COM1 through COM34 as DOS devices. This means that 'COPY *.* COM5' (assuming that the board is there and it is configured) would work through DOS. COMDRIVE is written to be used with IOtech's multi-port async boards.

To install COMDRIVE.SYS add the following line to your CONFIG.SYS file:

```
device=C:\COMDRIVE.SYS
```

(or the actual location of the program COMDRIVE.SYS.)

QCFG.EXE

This program is used to maintain the COMDRIVE device driver.

The port addresses of COMDRIVE are configurable and need to be defined before any multi-port board will operate properly with QMODE.COM and DOS. After the multi port board is installed into the PC, COMDRIVE.SYS needs to be configured to recognize it. To do this the base address of the installed multi-port board(s) needs to be known.

Let's assume that the multi-port board has a base address of 300H (default), and let's also assume that it is a COM232/4PC QUAD PORT board. This would put port 1 of the board at a base address of 300H,port 2=308H, port 3=310H, and port 4=318H. Lastly, assume standard COM1 and COM2 boards are already installed in the PC.

To get COM3 up and running enter 'COM3=300' from the command line of QCFG. This will pipe data that goes from DOS COM3 to IOtech's multi-port board port 1. Then, to get COM4 activated, the command 'COM4=308' needs to be issued from QCFG, and so on for all other ports that are available.

QMODE.COM

This utility is used to configure COM1-COM34. It operates like the DOS MODE command. To use QMODE the syntax is:

```
QMODE COMn[:]baud[,[parity][,[length][,[stopbits]
```

where:

n of COMn is 1 - 34 for the proper async logical port

baud: 110,150,300,600,1200,2400,4800,or 9600 (only first 2 characters required, ie. "96")

parity: E(ven) (default), N(one), O(dd)

length: 7 (default), 8

stopbits: 1 (default), 2

Example: QMODE COM18:2400,n,8,1

This command will configure logical COM address 18 to be 2400 baud, no parity, 8 bit, 1 stop bit.

1.11.1.1 Installing the Files

1. Add COMDRIVE to the CONFIG.SYS file

   `DEVICE=COMDRIVE.SYS`

2. Reboot, to recognize COMDRIVE.SYS

3. Run QCFG.EXE configure COMDRIVE.

   `COM3=300`

   :

4. Make sure, while in QCFG.EXE, to SAVE your modified configuration

   SAVE

   `Y` (answer yes to both questions)

   `Y`

:

5. Add QMODE commands to your AUTOEXEC.BAT for power-up configuration of the new COM PORTS

   `QMODE COM3:96,e,7,1`

6. Reboot.

7. Now all defined COM ports should be addressable.

   `'COPY *.* COM3'` will work properly

1.11.2 Windows Installation

To install the IOtech Windows 3.1 versions of the communications drivers, follow these steps:

1. Select `Run` from either File Manager or Program Manager. This is in the File Menu for either of these.
2. Type `a:\setup`. This works if your source diskette is inserted in drive A. Use the appropriate drive letter of the disk drive for your source diskette.
3. Setup will install the new device drivers and will modify the appropriate Windows system files. There is an additional application, Com Config, which is placed in the IOtech App group file.
4. Run the IOtech Com Config application. This will allow you to configure the device drivers for things such as the I/O address, IRQ, baud rate, handshaking, etc. This application incorporates context sensitive help.